What is claimed is:

1. A manufacturing process of a chip package, at least comprising:

providing a carrier which has a surface, a power pad and a ground pad, the surface of the carrier having a die bonding area, the power pad and the ground pad disposed on the surface of the carrier and outside the die bonding area;

disposing at least one passive component between the power pad and the ground pad, the passive component having at least two electrodes which are connected to the power pad and the ground pad respectively;

forming a metal layer on surfaces of the electrodes and exposed surfaces of the power pad and the ground pad;

disposing a die at the die bonding area on the surface of the carrier, the die having an active surface and a backside, the die having a plurality of die pads formed on the active surface; and

connecting two ends of at least one first conductive wire to one of the die pads of the die and to one of the electrodes of the passive component respectively.

2. The manufacturing process of claim 1, further comprising forming a dielectric material, the dielectric material covering the die, the passive component and the first conductive wire.

3. The manufacturing process of claim 1, wherein the carrier further has a signal pad, and the signal pad is disposed outside the die bonding area and farther from the die bonding area than the power pad and the ground pad.

4. The manufacturing process of claim 3, wherein the metal layer is formed on an exposed surface of the signal pad.

5. The manufacturing process of claim 3, further comprising connecting two ends of at least one second conductive wire to another one of the bonding pads of the die and to the signal pad respectively, the second conductive wire crossing over the passive component.

6. The manufacturing process of claim 5, further comprising forming a dielectric material, the dielectric material covering the die, the passive component, the first conductive wire and the second conductive wire.

7. The manufacturing process of claim 1, wherein prior to the step of disposing the passive component on the carrier, further comprising a step of forming a patterned solder mask layer on the surface of the carrier, the patterned solder mask layer exposing surfaces of the die bonding area, the power pad and the ground pad.

8. The manufacturing process of claim 1, wherein the metal layer is formed by electroplating.

9. The manufacturing process of claim 1, wherein the material of the metal layer is selected from a group consisting of nickel, gold and alloy thereof.

10. The manufacturing process of claim 1, wherein the passive component is selected from a group consisting of an inductor and a capacitor.

11. A manufacturing process of a package substrate, at least comprising:

providing a substrate;

forming a patterned conductive layer on a surface of the substrate, the patterned conductive layer having a power pad, a ground pad and a signal pad;

disposing at least one passive component between the power pad and the ground pad, the passive component having at least two electrodes which are connected to the power pad and the ground pad respectively; and

forming a metal layer on surfaces of the electrodes and exposed surfaces of the power pad, the ground pad and the signal pad.

12. The manufacturing process of claim 11, wherein after the step of forming the patterned conductive layer, further comprising the step of forming a patterned solder mask layer on the surface of the substrate, the patterned solder mask layer exposing surfaces of the power pad, the ground pad and the signal pad.

13. The manufacturing process of claim 11, wherein the material of the metal layer is selected from a group consisting of nickel, gold and alloy thereof.

14. The manufacturing process of claim 11, wherein the passive component is selected from a group consisting of an inductor and a capacitor.

15. A manufacturing process of a package substrate, at least comprising:

providing a substrate, comprising a surface and a plurality of bonding pads, wherein the bonding pads are disposed on the surface of the substrate;

disposing at least one passive component between the bonding pads, the passive component having at least two electrodes which are respectively connected to the bonding pads; and

forming a metal layer on surfaces of the electrodes and exposed surfaces of the bonding pads.

16. The manufacturing process of claim 15, wherein after providing the substrate, further comprising the step of forming a patterned solder mask layer on the surface of the carrier, the patterned solder mask layer exposing the surfaces of the bonding pads.

17. The manufacturing process of claim 15, wherein the metal layer is formed by electroplating.

18. The manufacturing process of claim 15, wherein the material of the metal layer is selected from a group consisting of nickel, gold and alloy thereof.

19. The manufacturing process of package substrate of claim 15, wherein the passive component is selected from a group consisting of an inductor and a capacitor.

20. A package substrate adapted to carry a die of a wire bonding type, the package substrate at least comprising:

a substrate having a surface, a power pad, a ground pad and a signal pad, wherein the surface of the substrate having a die bonding area, the power pad, the ground pad and the signal pad disposed outside the die bonding area;

at least one passive component disposed between the power pad and the ground pad, the passive component having at least two electrodes which are connected to the power pad and the ground pad respectively; and

a metal layer formed on exposed surfaces of the electrodes and exposed surfaces of the power pad, the ground pad and the signal pad.

21. The package substrate of claim 20, further comprising the step of forming a patterned solder mask layer on the surface of the substrate, the patterned solder mask layer exposing the surfaces of the power pad, the ground pad and the signal pad.

22. The package substrate of claim 20, wherein the material of the metal layer is selected from a group consisting of nickel, gold and alloy thereof.

23. The package substrate of claim 20, wherein the passive component is selected from a group consisting of an inductor and a capacitor.